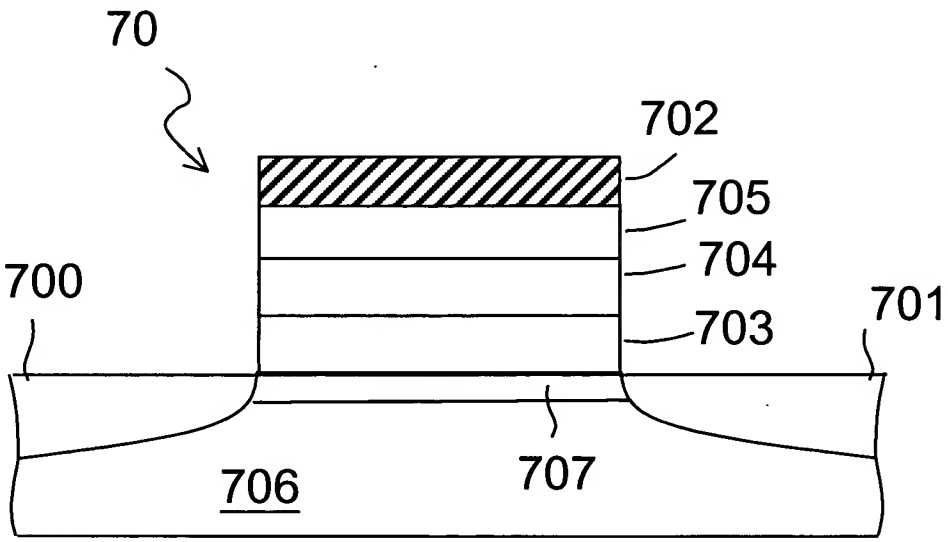


Fig. 1 (Prior Art)

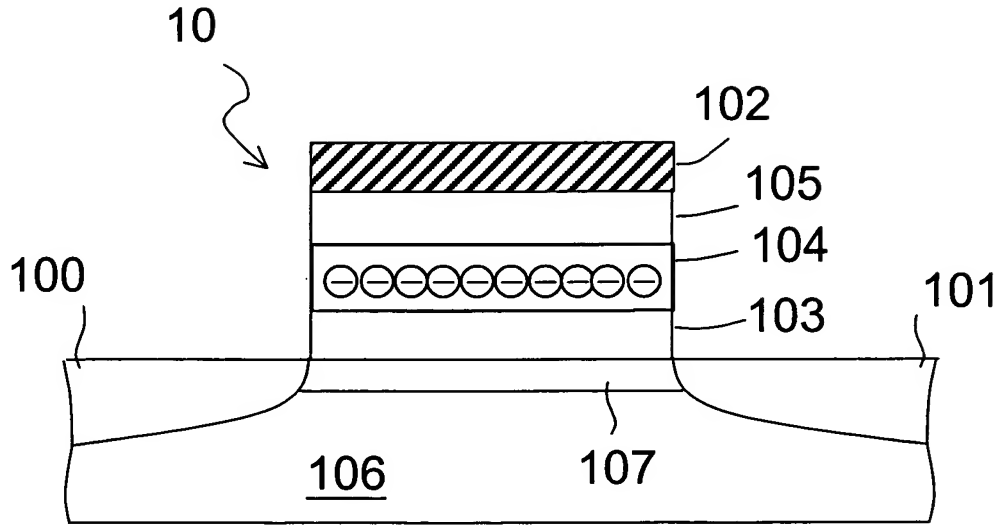


Fig. 2

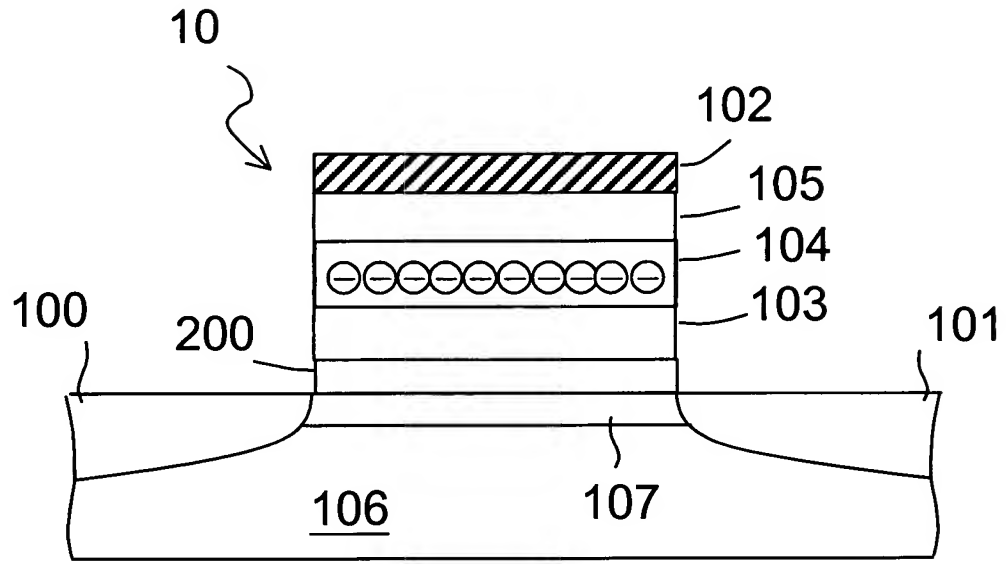


Fig. 3

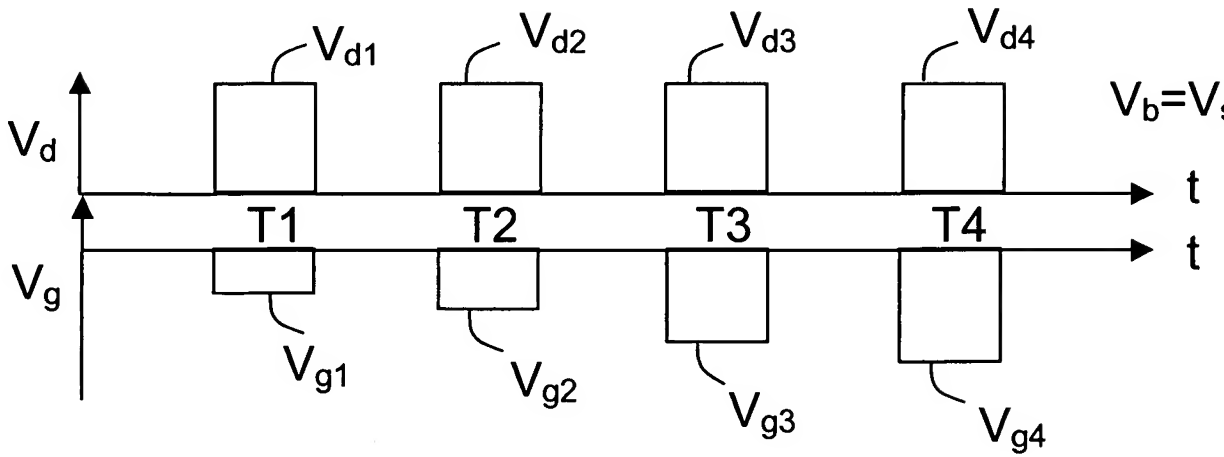

V_{d1}
V_{d2}
V_{d3}
V_{d4}
$V_b=V_s=0$
V_d
t
T1
T2
T3
T4
V_g
t
V_{g1}
V_{g2}
V_{g3}
V_{g4}

Fig. 4A

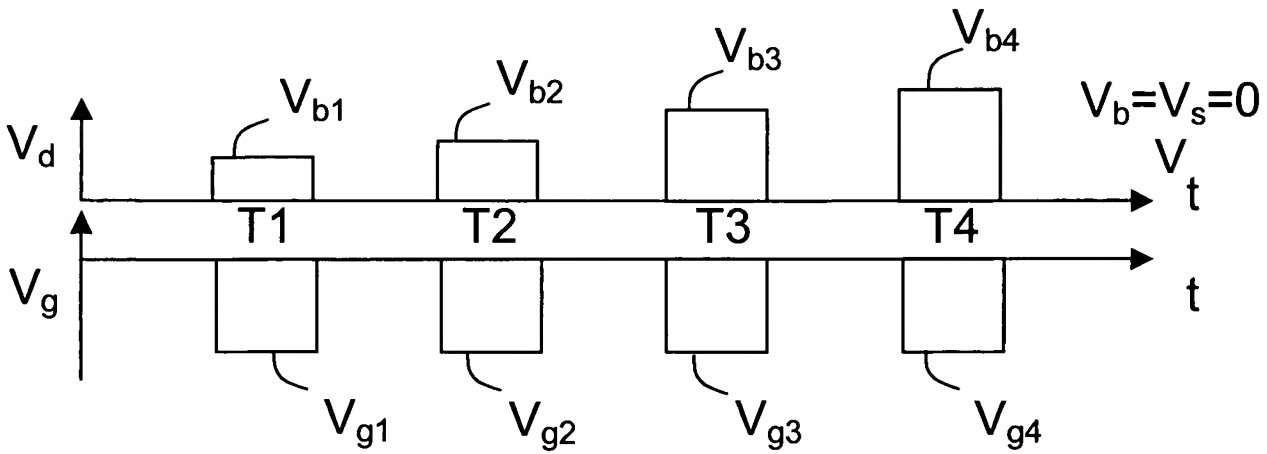

V_{b1}
V_{b2}
V_{b3}
V_{b4}
$V_b=V_s=0$
V_d
V
t
T1
T2
T3
T4
V_g
t
V_{g1}
V_{g2}
V_{g3}
V_{g4}

Fig. 4C

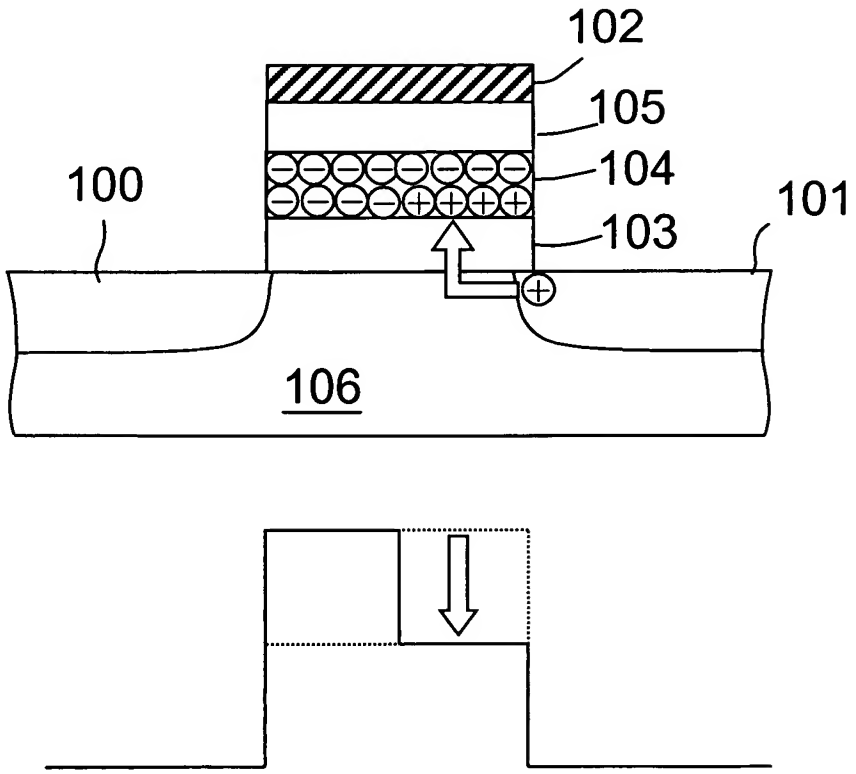


Fig. 4B

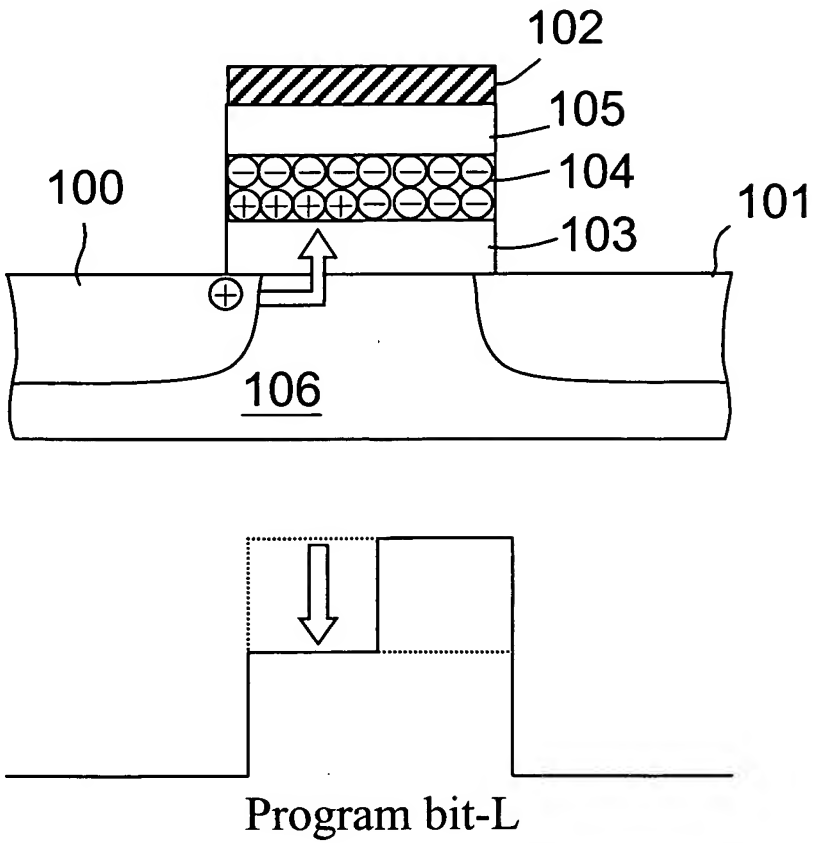


Fig. 4D

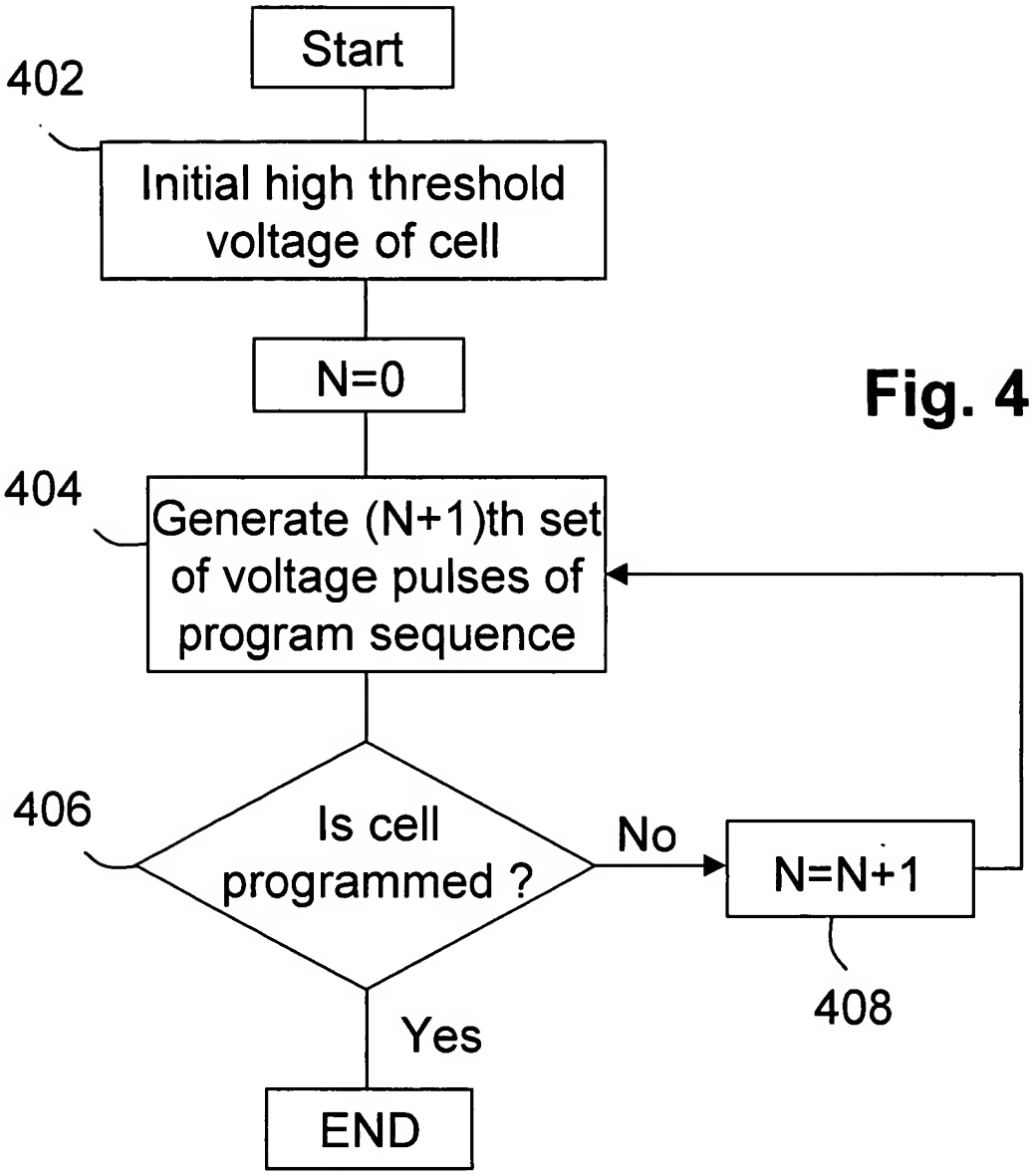

Start
402
Initial high threshold voltage of cell
N=0
404
Generate (N+1)th set of voltage pulses of program sequence
406
Is cell programmed ?
No
N=N+1
408
Yes
END

Fig. 4E

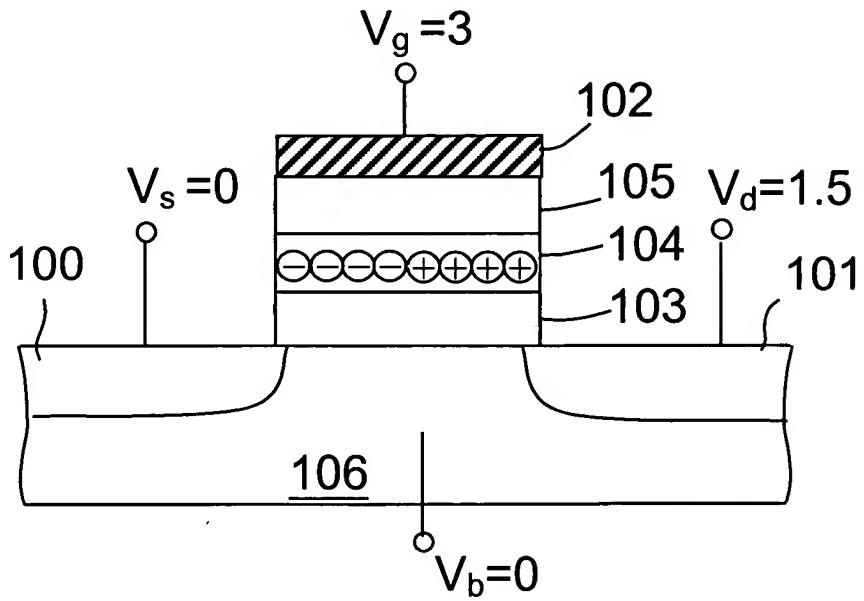


Fig. 5A

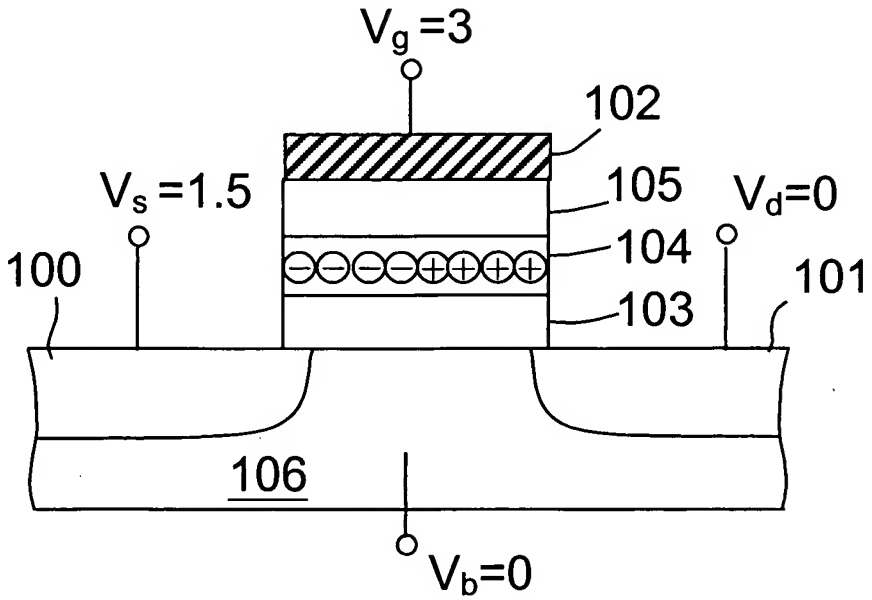


Fig. 5B

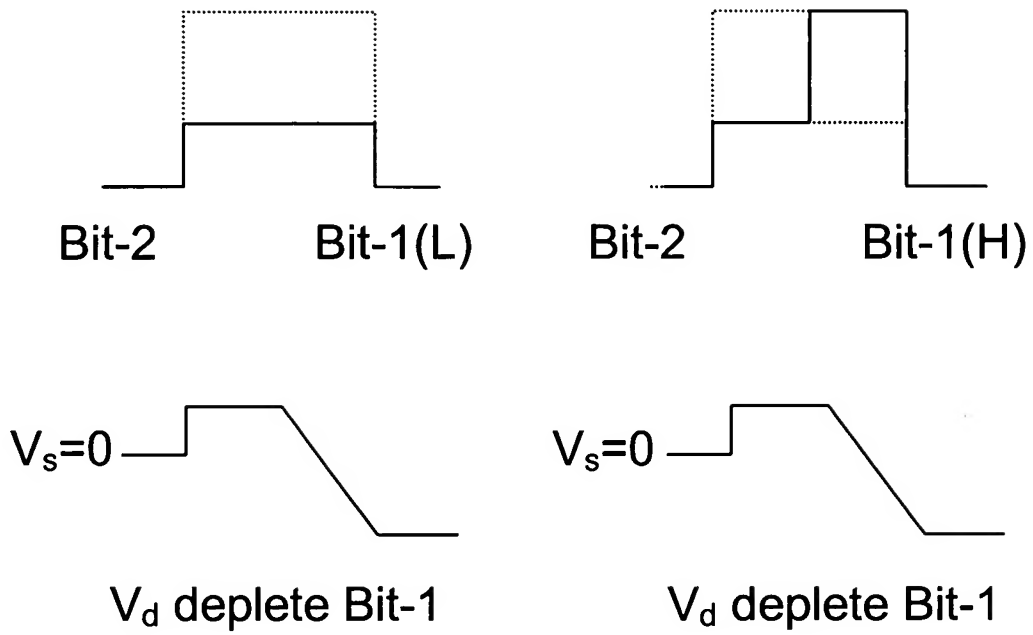
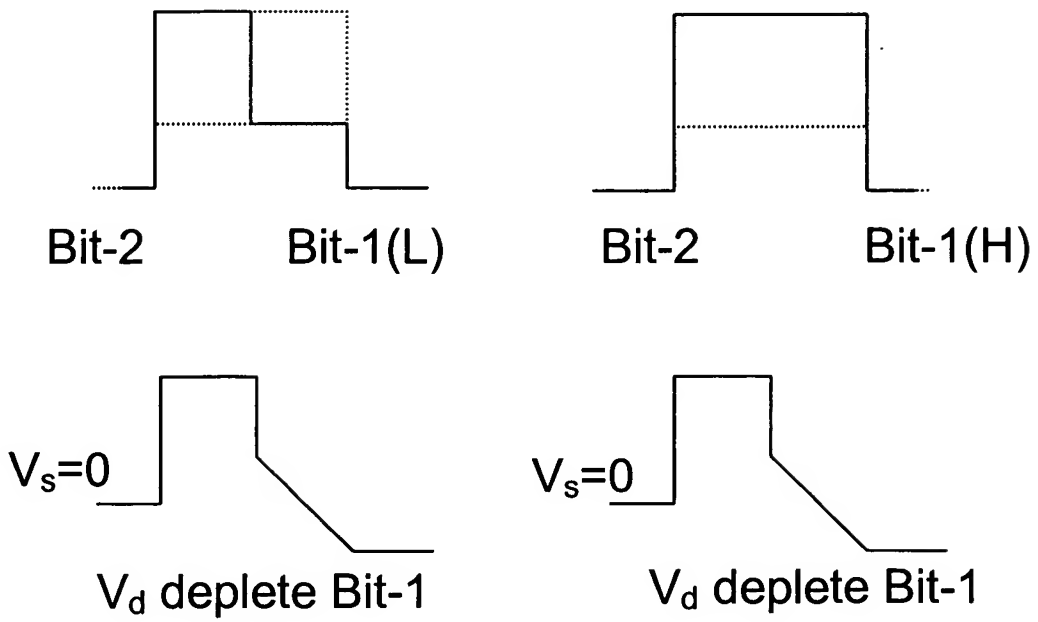
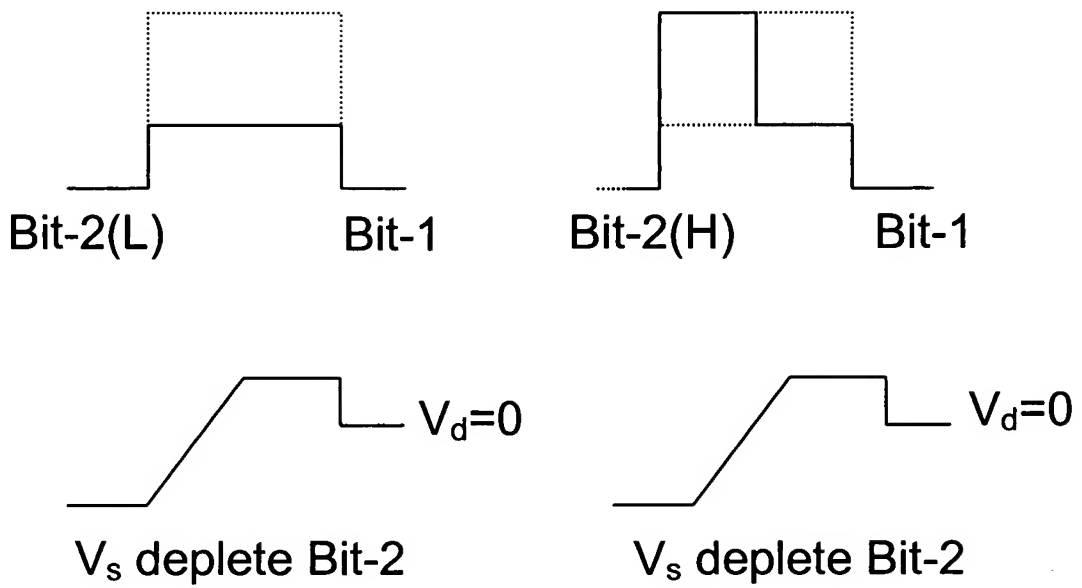

Bit-2
Bit-1(L)
Bit-2
Bit-1(H)
V_s=0
V_s=0
V_d deplete Bit-1
V_d deplete Bit-1
Read Bit 2 (low)

Fig. 6A



Read Bit 2 (High)

Fig. 6B



Read Bit 1 (low)

Fig. 6C

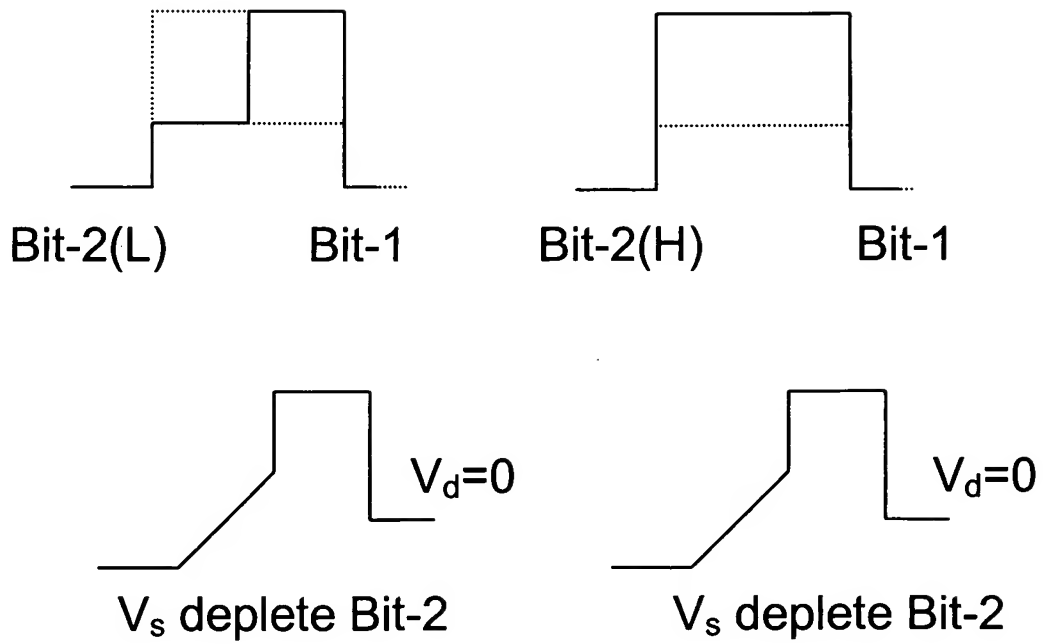

Bit-2(L)
Bit-1
Bit-2(H)
Bit-1
V_d=0
V_d=0
V_s deplete Bit-2
V_s deplete Bit-2
Read Bit 1 (high)

Fig. 6D

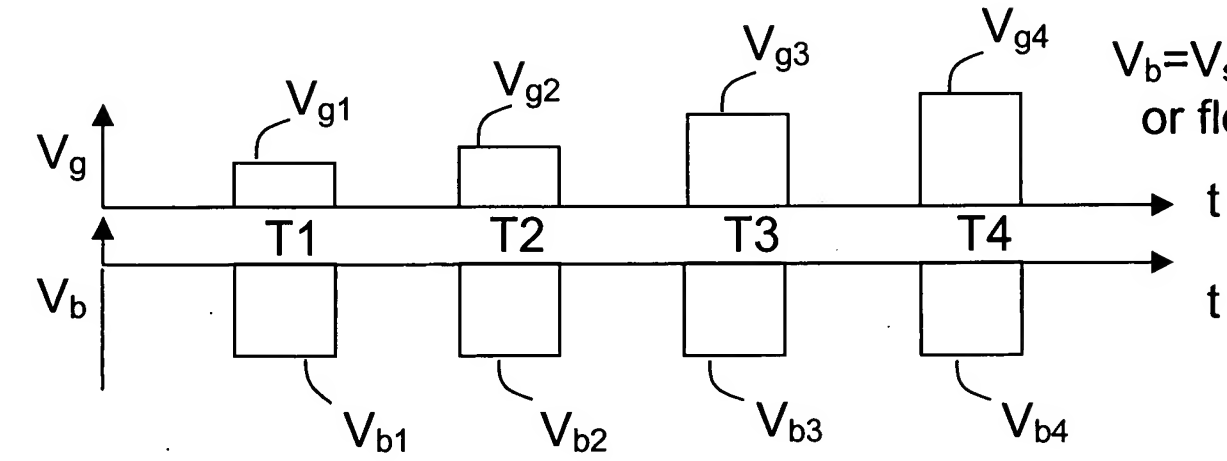

V_{g1}
V_{g2}
V_{g3}
V_{g4}
$V_b=V_s$= -10V
or floating
V_g
t
T1
T2
T3
T4
V_b
t
V_{b1}
V_{b2}
V_{b3}
V_{b4}

Fig. 7A

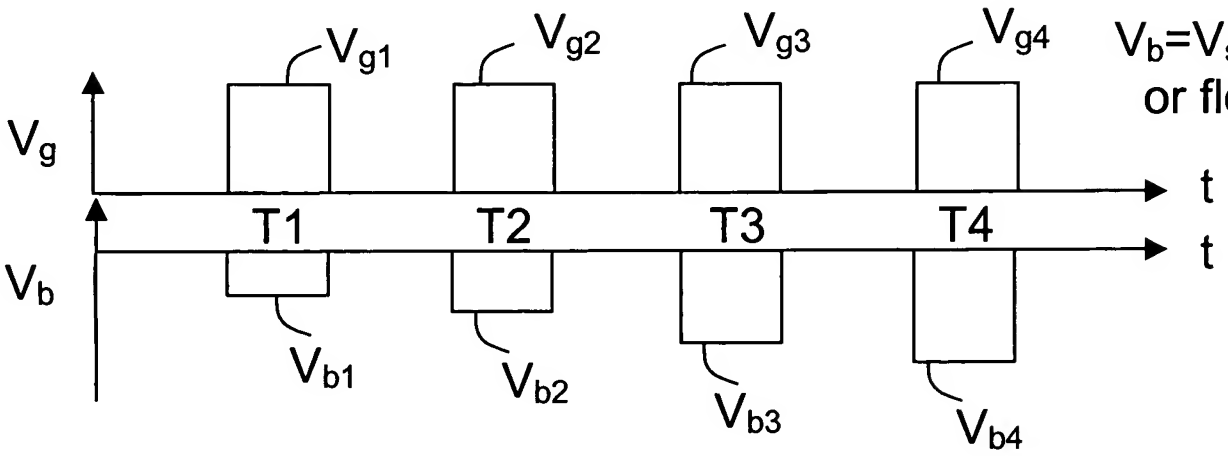

V_{g1}
V_{g2}
V_{g3}
V_{g4}
$V_b=V_s$= -10V
or floating
V_g
t
T1
T2
T3
T4
V_b
t
V_{b1}
V_{b2}
V_{b3}
V_{b4}

Fig. 7C

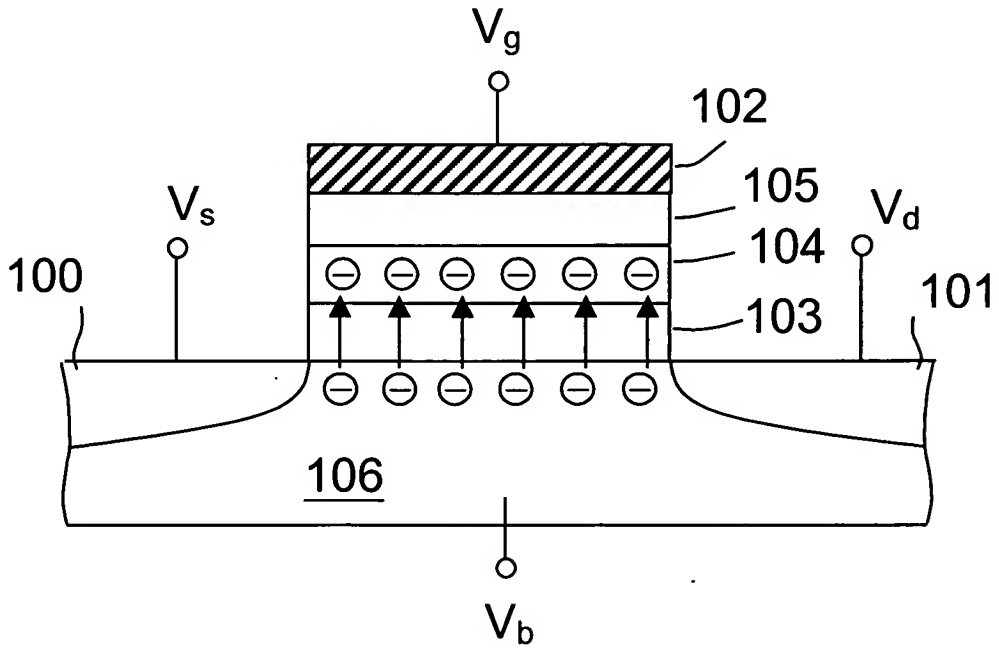


Fig. 7B

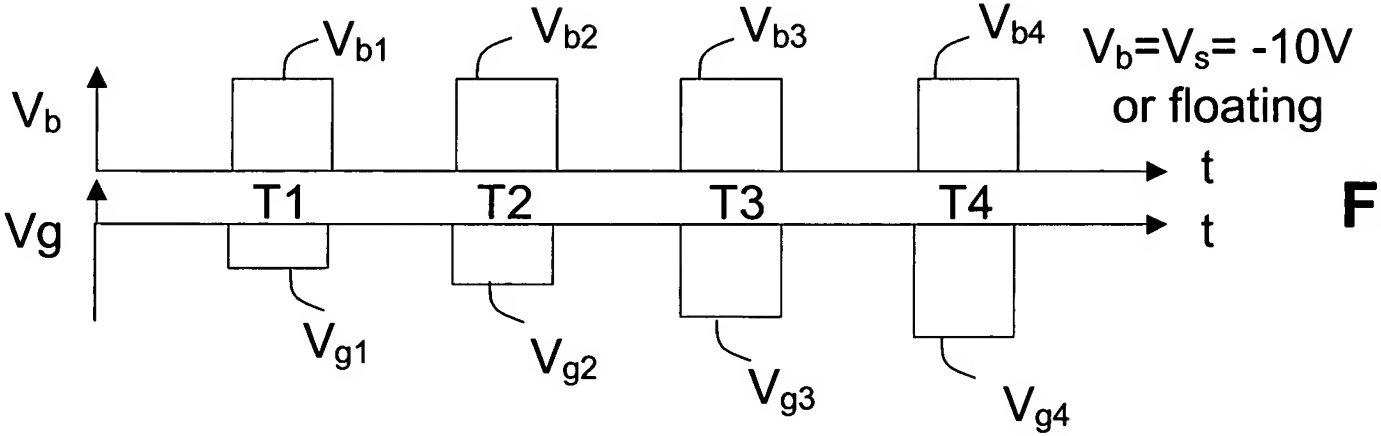

V_{b1}
V_{b2}
V_{b3}
V_{b4}
V_b=V_s= -10V
or floating
V_b
t
T1
T2
T3
T4
Vg
t
V_{g1}
V_{g2}
V_{g3}
V_{g4}

Fig. 7D

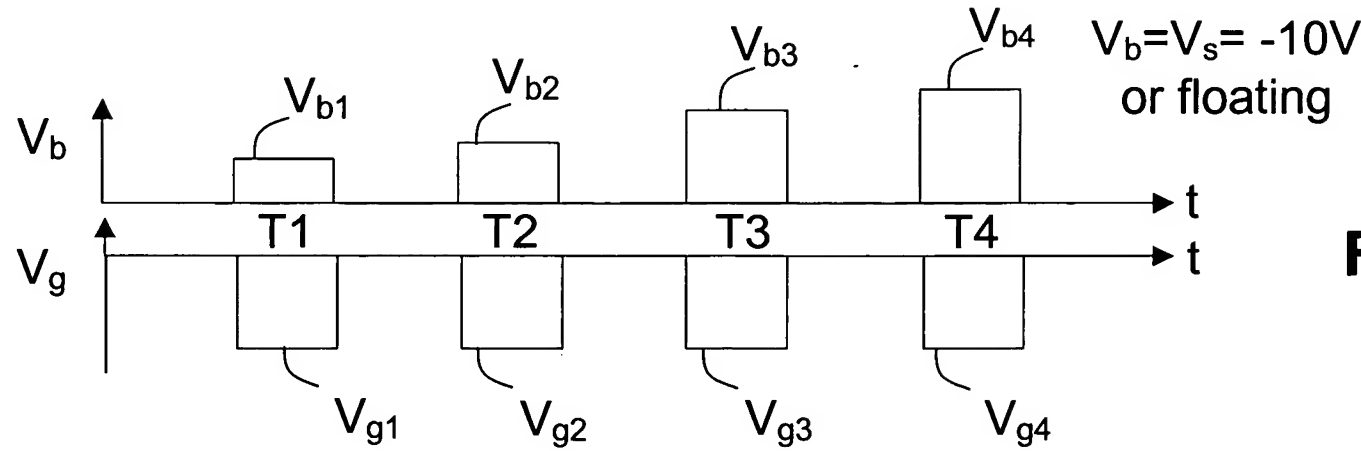
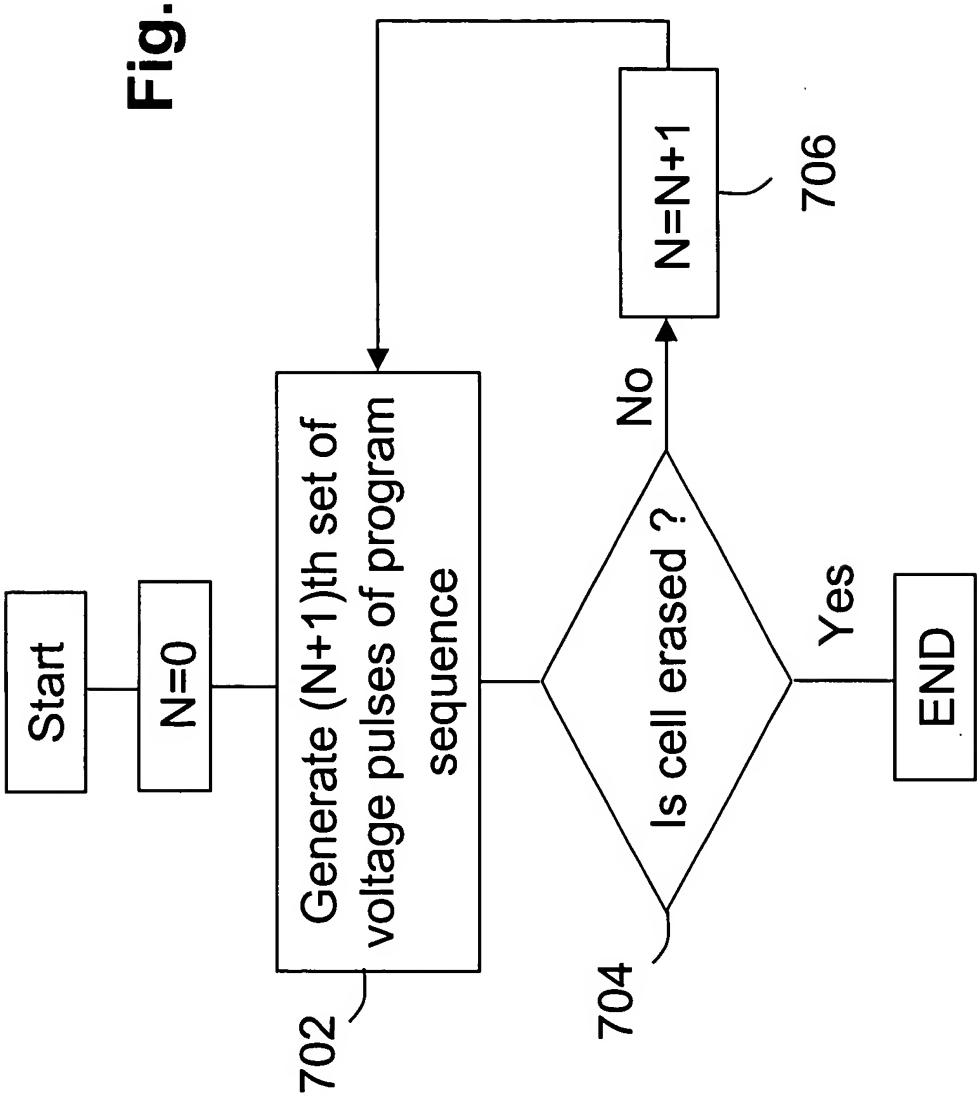

V_{b1}
V_{b2}
V_{b3}
V_{b4}
V_b=V_s= -10V
or floating
V_b
t
T1
T2
T3
T4
V_g
t
V_{g1}
V_{g2}
V_{g3}
V_{g4}

Fig. 7F

Fig. 7G


Start
N=0
Generate (N+1)th set of voltage pulses of program sequence
Is cell erased ?
No
Yes
N=N+1
END
702
704
706

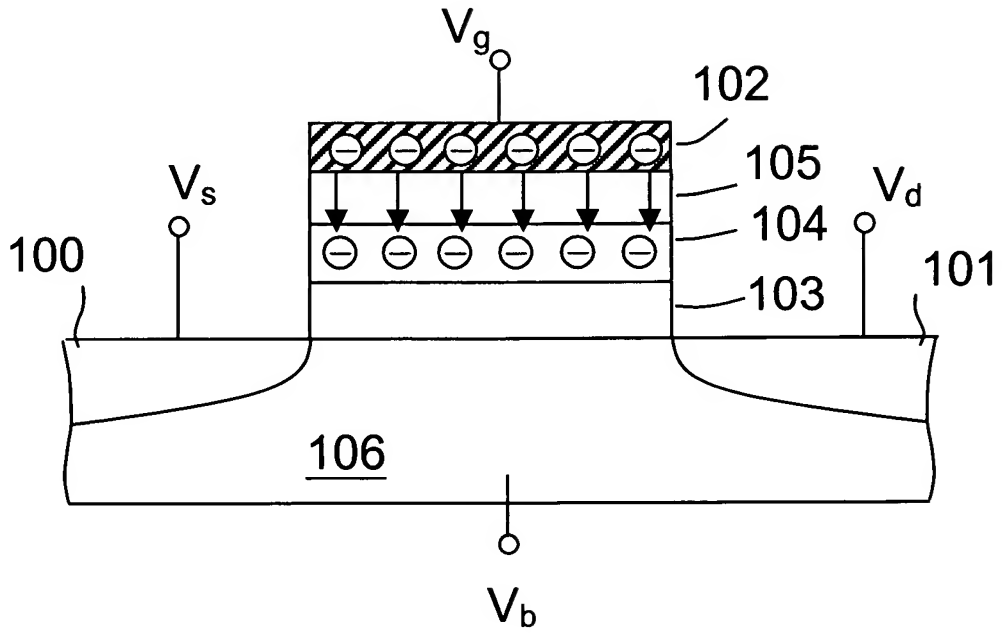


Fig. 7E

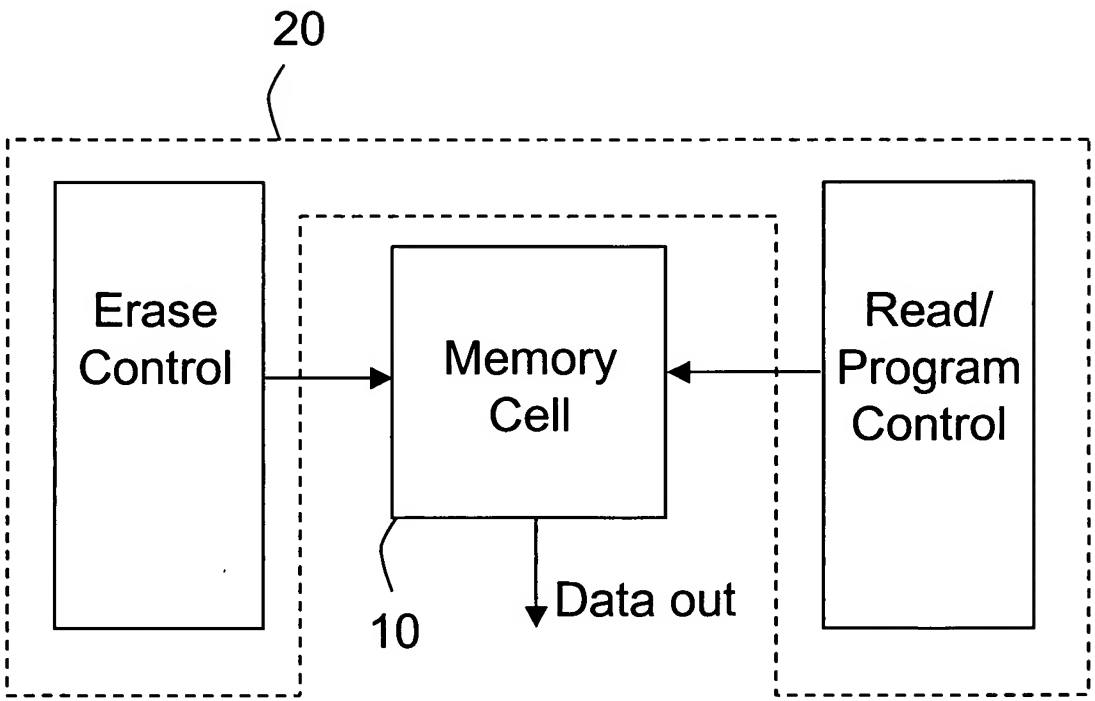

20
Erase Control
Memory Cell
Read/ Program Control
10
Data out

Fig. 8